ABSTRACT OF THE DISCLOSURE

In a cell library database, timing verification is conducted on an LSI which exists in a variable power supply system capable of changing the source voltage arbitrarily and which includes logic delay information associated with a plurality of source voltages. The database is configured, for example, so that the voltage information **V** of the source is represented in multiple bits **V [1:0]** and delay times Alh (Vlh) to Bhl (Vhh) between the time input signals **A** and **B** are each changed and the time the output signal **Y** changes are described for respective pieces of source voltage information LH (1.2 V), HL (1.5 V) and HH (1.8 V). This allows timing verification in the variable source system which operates with the source voltage changed dynamically.